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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/642,862 | 08/18/2003 | Vivek V. Gupta | VRT0092US | 3308 |

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| EXAMINER | |
|---|---|
| PATEL, HETUL B | |
| **ART UNIT** | **PAPER NUMBER** |
| 2186 | |

DATE MAILED: 05/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Advisory Action Before the Filing of an Appeal Brief | Application No. 10/642,862 | Applicant(s) GUPTA ET AL. | |
|---|---|---|---|
| | Examiner Hetul Patel | Art Unit 2186 | |

*--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

THE REPLY FILED on 20 April 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires *03* months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: *See Continuation Sheet*. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-36*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☒ Other: See Continuation Sheet.

Continuation of 3. NOTE: The proposed amenment(s) will not be entered because they raise new issues that would require further consideration and/or search.

Continuation of 13. Other: As to the remark, Applicant asserted that
(a) Kashima's CPU 11 is merely a different portion of what would be Kashima's upper-level system - not any sort of lower-level system at all.
(b) Kashima would require the lower level system operation of moving a data block from the lower level system to the disk cache 13 of the upper level system prior to allowing CPU 11 to complete its upper level system operation of transferring the data block from the disk cache 13 to the user buffer 14 in the main memory 12. Thus, Kashima's CPU 11 does not operate as a lower level system as claimed by Applicants.
(c) Applicants respectfully submit that a definition for the claimed "cloning information" can be found at paragraph (0023) of Applicants' original specification. Specifically, when "an upper-level system (e.g., a file system, a database application, a firmware module or the like) caches pages, those pages can be cloned into pages kept in a separate cache referred to herein as an old data cache" (Applicants' original specification, paragraph 0023, italics added for emphasis). Cloning refers to more than simply copying information from one place to another. Although cloning may comprise copying information as required by Applicants' dependent claim 3, cloning refers to preserving a version of data within a cache to avoid a read operation from a storage device to retrieve the required data. Thus, Applicants urge the Examiner to recognize the distinction between Applicants' claimed cloning operations and the common copying operations of Kashima.
(d) Applicants note that claim 36 specifically states that the "second cache comprises said second unit of storage." Applicants' respectfully submit that, despite being inapposite in either case, the Final Office Action remarks with respect to (c) and (d) are inconsistent because they equate Applicants' claimed second unit of storage with Kashima's disk array 1 rather than with Kashima's old data cache 17 as previously noted in the Final Office Action at page 3.
(e) The copying of Kashima is obviously different than Applicants' claimed cloning and fails to anticipate Applicants' claimed cloning because neither of Kashima's first and second caches that are maintained by the upper-level system are accessed by a lower-level system. Applicants urge the Examiner to recognize the distinction between Applicants' claimed cloning operations and the common copying operations of Kashima.
(f) Kashima clearly fails to teach, suggest, or otherwise disclose accessing a second cache by the lower level system when both the second and first caches are maintained by the upper level system.
(g) Kashima fails to provide features comparable to the claimed cloning. The claimed cloning is performed prior to information in the first unit of storage being modified, the first unit of storage being maintained by one of an upper-level system and a lower-level system; the second unit of storage being accessed by the other of the upper-level system and the lower-level system.
(h) Old data cache 17 of Kashima is not configured to be maintained by one of an upper-level system and a lower-level system, and accessed by the other of the upper-level system and the lower-level system.
(i) The Examiner has failed to address modifying Kashima in an attempt to support the cloning required by independent claim 36. Thus, no appropriate suggestion or motivation has been offered to modify Kashima as required to support a prima facie case of obviousness.
(j) Any modification to Kashima to show the cloning would not be based on Kashima's teachings or suggestion, but on Applicants' disclosure, which is improper hindsight.
(k) Applicants respectfully disagree with the Examiner that "a single cache comprising a plurality of caches" is admitted prior art, and Applicants hereby traverse the Examiner's assertion of Official Notice concerning such prior art.
(l) The Kashima system is incapable of providing any benefits by integrating multiple cache components on a single chip because Kashima must send all data to disk array 1, regardless of whether the data was initially from a single cache or multiple caches.

Examiner respectfully traverses Applicant's remark for the following reasons:

With respect to (a)-(b) and (h), First of all, Examiner would like to clarify the misunderstanding of equating the last limitation of claim 36 with Kashima prior art. Both the first cache and the first unit of storage of the current application are equated with Kashima's disk cache memory 13 in Fig. 4. Both the second cache and the second unit of storage of the current application are equated with Kashima's old data cache memory 17 in Fig. 4. The upper level system and the lower level system of the current application are equated with Kashima's main memory (12 in Fig. 4) and the disk array (2a-2d in Fig. 4), respectively. Therefore, the last limitation of claim 36 is equated as following: providing access to the second cache (i.e. the old data cache memory 17 in Fig. 4) by the other (i.e. the CPU 11 in Fig. 4) of the upper-level system (i.e. the main memory 12 in Fig. 4) and the lower-level system (i.e. the disk array 2a-2d in Fig. 4) (e.g. see the abstract and Fig. 4).

With respect to (c), Examiner would like to point out to Applicant that the paragraphs [0023] and [0063] of the specification of the current application pointed out by Applicant does not define the "cloning process". Applicant's quoted phrase from the specification, i.e. "an upper-level system (e.g., a file system, a database application, a firmware module or the like) caches pages, those pages can be cloned into pages kept in a separate cache referred to herein as an old data cache", does not define cloning process and does not prevent from equating cloning with copying. Furthermore, the definition of cloning as alleged by Applicant on pages 12-13 of the last response, i.e. "Cloning refers to ... to retrieve the required data", is not disclosed/supported by the original specification of this application. Therefore, Applicant's argument regarding the distinction between Applicants' claimed cloning operations and the common copying operations of Kashima is rendered moot.

With respect to (d) and (g), Examiner agreed with Applicant in the inconsistency between the response with respect to (c) and (d) in the remark section and the rejection of claim 36 in the Final rejection. This was due to a typographical error. Examiner really meant to equate the second unit of storage with Kashima's old data cache memory 17 in Fig. 4. Kashima does teach that the cloning (i.e. copying) process is performed prior to information in the first unit of storage (i.e. the disk cache 13 in Fig. 4) being modified, a first unit of storage being maintained by one of an upper-level system (i.e. the main memory 12 in Fig. 4) and a lower-level system (i.e. the disk array

2a-2d in Fig. 4), and second unit of storage (i.e. the old data cache memory 17 in Fig. 4) being accessed by the other (i.e. the CPU 11 in Fig. 4) of the upper-level system and the lower-level system (e.g. see the abstract and Fig. 4).

With respect to (e) and (f), Kashima discloses that the data held in the second cache (i.e. the old data cache memory 17 in Fig. 4) is sent to the lower-level system (i.e. the disk array 2a-2d in Fig. 4) during a write operation (see Kashima, col. 5, lines 32-37). In order to write the data into the lower-level system from the second cache, the data has to be read from the second cache; and in order to read the data from the second cache, the lower level system has to access (i.e. for reading) the second cache.

With respect to (i) and (j), the claim 36 is rejected based on 35 USC 102(b) as shown above. Therefore, Applicants' arguments regarding modification to Kashima, supporting a prima facie case of obviousness, improper hindsight etc. are rendered moot.

With respect to (k), Kashima teaches the computer (i.e. 10 in Fig. 8) having the main memory (i.e. 12 in Fig. 8) that comprises the first and second caches (i.e. 13 and 17 in Fig. 8) (e.g. see Fig. 8). However, Kashima does not clearly disclose that the first and second caches are a single cache. Integrating multiple components on a single chip reduces cabling problems, reduces latency required for communicating among multiple components, improves efficiency of message passing, reduces chip-to-chip communications costs, allows for less pin count, area saving and high speed data transfer between the elements and leads to further power efficiency and increased scalability. Because multiple caches integrated on a single cache (chip) provides improvements in efficiency, cost and scalability over individual caches, it would have been obvious to comprise a plurality of caches on a single cache. Therefore, the claimed invention would have been obvious to one of ordinary skill in the art at the time of the invention. Examiner introducing here the Merrell et al. (USPN: 5,829,038) reference and the Sne et al. (USPN: 5,890,207) reference just as evidence necessary to support the Examiner's conclusion of common knowledge (Official Notice) in the art in the previous Office Action mailed on February 15, 2006. Merrell et al. reference teaches the integrated hierarchical cache (i.e. 15 in Fig. 1) which includes a plurality of cache memories (i.e. L1-Ln) (e.g. see Fig. 1). Sne et al. reference also teaches the integrated cache memory (i.e. the global memory) comprising the plurality of memories (e.g. see Col. 5, lines 62-65).

With respect to (l), Examiner agreed with Applicant that in the Kashima's system, all data must be sent to the disk array 1 regardless of whether the data was initially from a single cache or multiple caches. However, instead of writing the data from the first cache to the second cache (which is located off-chip, i.e. not integrated on the same chip as the first cache) and to the disk array in parallel, by having the first and second cache integrated on the same chip, data can be quickly written/transferred from the first cache to the second cache to free-up the first cache for the new data and then transferring the data from the second cache to the disk array later on..

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